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Archinteriors vol. 31 includes 10 fully textured oriental style interior scenes. The scene is ready for V-RayÃ . Archinteriors vol 3 Download [e31cf57bcd] Free. evermotion archinteriors vol 31 0 1 2 3 4 5.1. Field of the Invention The present invention relates to the field of technology for silicon on insulator (SOI) chips. More specifically, the present invention relates to a method of forming a device with an edge termination for an SOI chip. 2. Related Art Silicon on insulator (SOI) circuits offer several advantages over bulk silicon circuits. One advantage is the reduced capacitance from the substrate (or bulk silicon) to the floating body of the transistor, thus resulting in a large performance boost for the device. Another advantage is that SOI circuits reduce latch-up. Latch-up is a phenomenon that can result in the creation of a parasitic bipolar junction transistor (BJT) between the P-N junction formed by the buried oxide (BOX) layer in the SOI chip and the P-N junction of the active silicon layer. In the case of the buried oxide (BOX) being formed of silicon, the P-N junction of the active silicon layer is floating and therefore can be forward biased. The forward biased active P-N junction can unintentionally turn on the parasitic BJT causing latch-up. In the manufacture of SOI chips, a buried oxide (BOX) layer is grown on a silicon wafer. Next, a silicon active layer is deposited over the BOX layer. Then a patterning step is performed to remove portions of the silicon active layer, leaving a patterned silicon active layer. Next, an edge isolation region is formed around the peripheral edge of the silicon active layer leaving the BOX layer exposed and exposed to the backside of the wafer. Next, the backside of the wafer is thinned, resulting in a thinned wafer. The thinning step is performed until the silicon active layer and the edge isolation region are exposed. A conventional manufacturing process for SOI transistors is described in T. Shimizu et al., "New Scheme of Active Isolation of SOI CMOSFETs," Japanese Journal of Applied Physics, Vol. 39 (2000) pp. 6243-6248. See also, T. Shimizu et al., "New Lateral SOI Insulator Isolation Technique: 3-D BOX