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Samuraijack (Samurai X) is the main protagonist in the Samuraijack television series. As with the title character, the series also has a mythology, with warring factions and parallel dimensions. □□□ □□□□□ □□

SamuraiJack_Dylan_Walker_1.jpg See also: SamuraiJack: Code of the Samurai 2 #1265 - SamuraiJack: Code of the Samurai 2 SamuraiJack: Code of the Samurai 2! #9331 - SamuraiJack: Code of the Samurai 2! Everest, Tibet, and the Indian subcontinent: A History of Exploration in the Nineteenth CenturyThe present invention is directed to integrated circuits and their processing for the manufacture of semiconductor devices. More particularly, the invention provides a method and system for semiconductor chip trimming and design rule checking. Merely by way of example, the invention has been applied to microlithography processing. But it would be recognized that the invention has a much broader range of applicability. For example, the invention can be applied to integrated circuits (ICs) and other electronic components, micro-electromechanical systems (MEMS), and the like. In the fabrication of semiconductor integrated circuits, there is a constant desire for higher device density, high reliability, and high manufacturing throughput. To achieve these ends, complicated integrated circuit designs are usually created in the first place. These designs are then fabricated into semiconductor chips. Each semiconductor chip often requires numerous integrated circuit patterns to achieve a desired functional specification. The patterns that comprise the integrated circuit designs are laid out by a designer in an abstract design layout tool. The abstract design layout tool usually creates a floor plan or layout of the chip. The floor plan illustrates the various components for the semiconductor chip. But the overall integrated circuit chip layout must be further converted into a physical layout image or design layout file for fabrication. The floor plan or abstract design layout tool is typically an abstracted representation of the physical layout on a wafer or mask. The design layout file is then used to mask fabrication processes. Multiple mask levels are generally used to form the integrated circuit chip. Such mask levels include the mask 1 for manufacturing the wafer, mask 2 for manufacturing the mask used to pattern the wafer, mask 3 for manufacturing the masks used to pattern subsequent layers

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